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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,064	12/09/2003	Zvi Or-Bach	38897-199163	2943

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EXAMINER	
QUACH, TUAN N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,064	OR-BACH ET AL.	
	Examiner	Art Unit	
	Tuan Quach	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 and 3-12 are elected without traverse.

The abstract of the disclosure is objected to because it appears to correspond to the non-elected invention of claim 2, namely the method of fabricating the semiconductor device as opposed to the semiconductor device in claims 1 and 3-12. Correction is required. See MPEP § 608.01(b).

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 3-8 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10, 27-29, 61, 62 of copending Application No. 10/321,669 ('669). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Instant claim 1 corresponds to claims 1 and 10 of '669: the borderless logic array and areas I/O, configurable I/O comprising at least one metal layer that is the same for all I/O configurations correspond to claims 10 and 5 of "669 and since the use of at

least one metal that is same for all configurations would have been obvious as in claim 5 wherein at least one metal layers comprise substantially repeating pattern used for interconnections.

Instant claim 3 corresponding to claim 1 of '669 including the borderless logic array and the redistribution layer therein wherein the repeating module containing logic cells and I/O cells corresponds to the repeating modules in claim 9. Regarding claims 4 and 5, the arrangement of I/O cells in spaced parallel lines of desired spacing would have been obvious.

Regarding claims 6-8, the repeating module comprising at least two metal layers including repeating patterns would have been obvious over claims 6 and 7 of '669.

Claims 9-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10, 27-29, 61, 62 of copending Application No. 10/321,669 ('669) in view of Hively et al. or Cox.

Claims 9 and 10 differ from the claims of '669 as delineated above primarily in that the additional custom layer or layers for desired applications are not delineated. Claims 11 and 12 only require the semiconductor device comprising repeating I/O cells wherein the cells are customized using only custom via layers are not patentable in that the semiconductor device comprising the repeating I/O cells have been claimed in '669, e.g., claims 1, 9, 10, and since these are product claims wherein the intended use would have been obvious or apparent for the reasons delineated below. A recitation directed to the manner in which a claimed apparatus is intended to be used does not distinguish the claimed apparatus from the prior art – if the prior art has the capability to

so perform. See MPEP 2114 and *Ex parte Masham,* 2 USPQ2d 1647 (1987). The recitation of a new intended use for an old product does not make a claim to that old product patentable. *In re Schreiber*, 44 USPQ2d 1429 (Fed. Cir. 1997). Such use of the customized layers would have been further conventional and obvious as evidenced below.

Additionally, Hively et al. (5,514,884) teaches the provision of customized via layers to achieve advantages including avoidance of blocks of circuitry, defective control logic, defice bus line, and to select the organization of the final structure. See column 3 lines 25 to column 4 line 50, particularly column 3 lines 51 to column 4 line 11.

Cox 6,693,454 teaches customization using via layer masks wherein at least some of the plurality of the metal layers are customed and used to configure the device for specific application. See column 2 lines 2-41, line 60 to column 6 line 56, particularly column 6 lines 28-36, lines 50-56.

It would have been obvious to one skilled in the art to have employed in the invention claimed in '669 employing additional custom layers since such is conventional and advantageous as evidenced by Hively et al. or Cox to obtain the desired applications.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy taken with Sivilotti et al.

Regarding claim 1, Shenoy 5,994,766 teaches the logic array comprising repeating core and at least one of area of I/Os being configurable, e.g., Fig. 1, column 4 line 66 to column 5 line 11 wherein the I/0 slots are arranged in linear arrays of cells or titles and wherein the repeating core correspond to the one or more logic circuit and associated I/0. Shenoy lacks primarily the recitation of the borderless array and the same metal in all the configuration.

Sivilotti et al., 6,316,334 B1 teaches the use of borderless arrays which can be cut to prevent substantial waste. See column 1 line 50 to column 2 line 24.

It would have been obvious to one skilled in the art in practicing the Shenoy invention to have employed borderless array since such is conventional and advantageous to prevent substantial waste as suggested by Sivilotti et al. The use of a at least one metal which is the same for all I/O configuration would have been obvious

corresponding to the processing step as opposed to a structural difference; the use of the same metal layer would have been further obvious and advantageous wherein the same metal layer can be patterned in the same step or using the same masking, as opposed to using different metal layer for different I/O. Such would have been further obvious as evident in Sivilotti et al., column 3 lines 53-62.

Regarding claim 3, Shenoy teaches a semiconductor device comprising a logic array 19/100, areas I/Os 26, redistribution layer 108 for redistributing at least some of said are I/Os. See column 4 line1 to column 8 line 20. Athough Shenoy does not recite the borderless array, such would have been conventional and obvious as evidenced by Sivilotti et al. as delineated above. The arrangement of I/O cells in desired patterns and suitable spacing as in claims 4 and 5 is well within the purview of one skilled in the art and as evidenced by Shenoy above, and as such would have been obvious.

Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy taken with Sivilotti et al. as applied to claims 1, 3-5, above, and further in view of the IBM TDB publication 6/86, Vol. 29, No. 1, pp. 88-94 (Multi-function FET I/O Masterslice cell) and Cox.

Regarding claims 6-8, the use of at least two metal layers for the repeating pattern would have been obvious since Shenoy further shows at least one pad 52 used to connect the semiconductor device to other devices overlays at least a portion of the logic array or a portion of area I/Os, column 7 lines 64-66 and as evidenced by the IBMTDB article, Fig. 3, and the associated disclosure wherein at least one metal layer

M(1), and including two metal layers M(1) and M(2) can be employed for all I/O configurations. Such would have been further obvious as evidenced by Cox 6,693,454 which teaches customization using via layer masks wherein at least some of the plurality of the metal layers are customized and used to configure the device for specific application, thereby permitting the same metal layers being employed. See column 2 lines 2-41, line 60 to column 6 line 56, particularly column 6 lines 28-36, lines 50-56.

Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy taken with Sivilotti et al. and the IBM TDB article or Cox as applied to claims 6-8 above and further in view of Hively.

The references are applied as above including the repeating I/O cells in claims 11 and 12 are delineated above, including in Shenoy and as evidenced in Sivilotti et al., Fig. 3, 8, column 3 line 2 to column 4 line 3. These references do not recite the customized layers.

Additionally, Hively et al. (5,514,884) teaches the provision of customized layers to achieve advantages including avoidance of blocks of circuitry, defective control logic, defective bus line, and to select the organization of the final structure. See column 3 lines 25 to column 4 line 50, particularly column 3 lines 51 to column 4 line 11.

Cox 6,693,454 is applied as above and teaches customization using via layer masks wherein at least some of the plurality of the metal layers are customized and used to configure the device for specific application. See column 2 lines 2-41, line 60 to column 6 line 56, particularly column 6 lines 28-36, lines 50-56.

It would have been obvious to one skilled in the art to have employed in the invention above to have employing additional custom layers since such is conventional and advantageous as evidenced by Hively et al. or Cox to obtain the desired applications.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rostoker et al. 5,264,729, and How et al. 6,613,611 B1 are made of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Quach whose telephone number is (571) 272-1717. The examiner can normally be reached on M - F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562.

Tuan Quach
Primary Examiner